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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,856	02/19/2004	Yasushi Inagaki	041226-0307277	2465

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,856	INAGAKI ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,9,10,15 and 79-93* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,10,15,79-90,92 and 93* is/are rejected.

7)☒ Claim(s) *91* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 15, 79, 83-85 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamashita, as in the record

As to claim 15, Yamashita discloses a printed circuit board as shown in figure 1G constituted by alternately laminating insulating layers and conductive circuits, see figure 1G on a core substrate containing a ceramic capacitor (10, an insulating material of the capacitor 10 inherently made by ceramic), the capacitor (10) having first and second electrodes (12), wherein the core substrate containing said capacitor (10) comprises a first resin substrate (on top of sealling layer 30), a second resin substrate (20) having an opening (21) and a third resin substrate (a bottom layer formed on bottom surface of the layer 20) in a multilayer manner while interposing bonding plates, said first resin substrate and said ceramic capacitor (10) are coupled to each other by an insulating

bonding agent (sealing layer 30) and having a coefficient of thermal expansion (CTE) lower than a CTE of the first substrate and connected to the electrode (12) of the capacitor, and a via hole (40), through which the conductive pad is connected to the conductive circuit on the core substrate, is formed in the first resin substrate.

As to claim 79, Yamashita further comprising a metal film (51) formed on the electrode of said capacitor (10).

As to claims 83-85, Yamashita further comprising a plurality of bumps (column 6, lines 9-26) formed on an outer layer of the insulating layers and constituting a bump area, wherein at least one of the bumps is electrically connected to the electrode of the capacitor through a via hole formed immediately below the bump area, and an IC chip (60) is to be mounted on the bump area.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 5, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mowatt et al. (U.S. Patent 6,306,670) in view of Yamashita (U.S. Patent 5,875,100).

As to claims 1, 4-5, Mowatt et al. discloses a printed circuit board as shown in figures 4-6 comprising:

a core substrate comprising first and second resin substrates (10; (126, 138, 150)), the second resin substrate (10) having a plurality of openings (14, 24) and a third resin substrate (element 16 located at a bottom of the substrate 10, see figure 6) in a multilayer manner while interposing bonding plates, the opening covered with the second surface of the first resin substrate;

insulating layers and conductive circuit layers (these elements formed in the substrates (138, 150) and laminated on top of a first surface of layer 126 alternately laminated on the core substrate;

a semiconductor die (56) formed in the opening (14) of the second resin substrate (10);

first and second conductive pads (130, 132) formed on (and in) a surface of the first resin substrate and connected to electrodes (60, 62) of the die, see figure 6;

first and second via holes (the vias include conductor 142, 144) formed in the first resin substrate, directly connected to the first and second conductive pad and conductive circuits.

Mowatt et al. does not specific disclose the semiconductor die (56) specifically being a capacitor made of ceramic and having external electrodes.

Yamashita shows a PCM (multilayer board) comprising a semiconductor chip (10, column 2, line 67), which is a capacitor (column 4, line 67 through column 5, line 2) formed in the opening (21) of the second resin substrate (20), the capacitor (10) having first and second electrodes (12).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a capacitor as taught by Yamashita employed the die of Mowatt et al. for the purpose of storing power for the multilayer circuit board.

As to claim 9, Yamashita further comprising metal films (51) formed on the electrode of said capacitor (10) and contact with first and second pads (noted: figure 1G shows the metal film 51 electrical connected to the pads (where the chip 60 connected to)).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a capacitor having a metal film as taught by Yamashita employed the die of Mowatt et al. for the purpose of providing electrical connection.

5. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mowatt et al. in view of Yamashita, and further in view of Sakaguchi et al. (5,837,624).

Regarding claims 2-3, Mowatt et al. and Yamashita disclose all of the limitations of the claimed invention, except for each of said bonding plates having said first, second and third resin substrates having a core made of glass cloth and a resin impregnated with a thermosetting resin.

Sakaguchi teaches a printed wiring board as shown in figures 1-5 comprising an insulating material having a core made of glass cloth and a resin impregnated with a thermosetting resin.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have an insulating material having a core made of glass cloth

and a resin impregnated with a thermosetting resin as taught by Sakaguchi employed in one of the substrates of the PCB of Mowatt and Yamashita in order to provide a CTE mismatch and flexure on the PCB.

6. Claims 2-4, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mowatt et al. in view of Yamashita, and further in view of Ehman et al. (U.S. Patent 6,021,050).

As to claims 2-4, Mowatt et al. and Yamashita disclose all of the limitations of the claimed invention, except for each of said bonding plates having said first, second and third resin substrates having a core made of glass cloth and a resin impregnated with a thermosetting resin, and a plurality of openings and capacitors formed in the openings.

Ehman et al. teaches a printed wiring board as shown in figures 1-3 comprising layers (12, 14, and 16) each made of glass cloth and a resin impregnated with a thermosetting resin.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have layers made of glass cloth and a resin impregnated with a thermosetting resin as taught by Ehman employed in one of the substrates of the PCB of Mowatt and Yamashita in order to provide a CTE mismatch and flexure on the PCB.

As to claims 10, Mowatt and Yamashita disclose all of the limitation of the claimed invention, except for the metal film formed on the electrode of said capacitor is a plated film mainly consisting of copper.

Ehman teaches copper conductor circuit paths 30, 32 formed on a surface of the capacitor 26.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have copper path formed on the capacitor as taught by Ehman employed in one of the substrates of the PCB of Yamashita in order to provide good electrical conductivity.

7. Claims 81-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita in view of Sakaguchi et al. (5,873,624).

Regarding claims 81-82, Yamashita discloses all of the limitations of the claimed invention, except for each of said bonding plates having said first, second and third resin substrates having a core made of glass cloth and a resin impregnated with a thermosetting resin.

Sakaguchi teaches a printed wiring board as shown in figures 1-5 comprising an insulating material having a core made of glass cloth and a resin impregnated with a thermosetting resin.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have an insulating material having a core made of glass cloth and a resin impregnated with a thermosetting resin as taught by Sakaguchi employed in one of the substrates of the PCB of Yamashita in order to provide a CTE mismatch and flexure on the PCB.

8. Claims 80-82, and 86-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita in view of Ehman et al. (U.S. Patent 6,021,050).

As to claims 81-82, and 86-90, Yamashita discloses all of the limitations of the claimed invention (see noted in claim 15 for the structure of the capacitor 10), except for each of said bonding plates having said first, second and third resin substrates having a core made of glass cloth and a resin impregnated with a thermosetting resin, and a plurality of openings and capacitors formed in the openings.

Ehman et al. teaches a printed wiring board as shown in figures 1-3 comprising layers (12, 14, and 16) each made of glass cloth and a resin impregnated with a thermosetting resin.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have layers made of glass cloth and a resin impregnated with a thermosetting resin as taught by Ehman employed in one of the substrates of the PCB of Yamashita in order to provide a CTE mismatch and flexure on the PCB.

As to claim 80, Yamashita discloses all of the limitation of the claimed invention, except for the metal film formed on the electrode of said capacitor is a plated film mainly consisting of copper.

Ehman teaches copper conductor circuit paths 30, 32 formed on a surface of the capacitor 26.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have copper path formed on the capacitor as taught by Ehman

employed in one of the substrates of the PCB of Yamashita in order to provide good electrical conductivity.

9. Claims 92-93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita in view of Ehman, and further in view of Suzuki (all the references cited in the record).

Yamashita as modified by Ehman discloses all of the limitations of the claimed invention except for the pad and electrode of the capacitor are connected via a conductive adhesive.

Suzuki shows a hybrid module as shown in figure 10 comprising a conductive adhesive seal (8) via connected to a pad (where the chip 11 formed on) and an electrode of the capacitor.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Suzuki employed in the PCB of Yamashita and Ehman in order to provide an electrical connection.

Allowable Subject Matter

10. Claim 91 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. Applicant's arguments with respect to claims 1-5, 9-10, 15, 79-93 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues:

Mowatt et al. in view of Yamashita does not disclose a chip capacitor having external electrodes.

Examiner disagrees because the chip (10) which utilizes as a capacitor having external electrodes (12).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan Dinh
May 22, 2007.

TUAN T. DINH
PRIMARY EXAMINER